

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kerry Bernstein, et al.

Examiner: Unassigned

Serial No: 10/6041791

Art Unit: Unassigned

Filed: 6/30/03

Docket: BUR920010207US1 (15821)

For: METHODOLOGY FOR FIXING Qcrit
AT DESIGN TIMING IMPACT

Dated: June 16, 2003

Commissioner for Patents
United States Patent and Trademark Office
Alexandria, Virginia 22313-3513

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

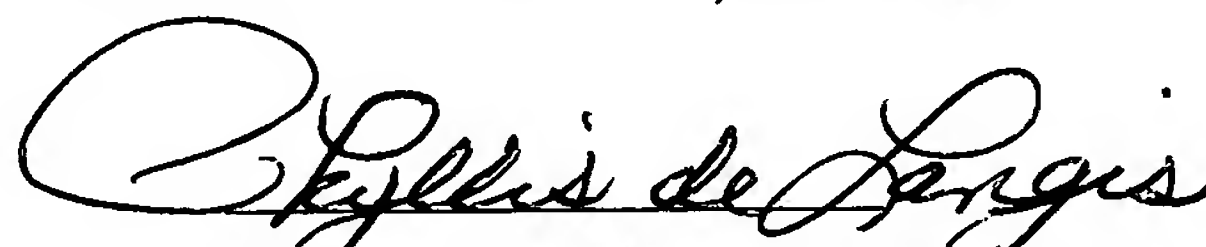
In accordance with 37 C.F.R. §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Chan, "Technique for Reducing Personalized Array Soft Errors", RESEARCH DISCLOSURE, Kenneth Mason Publications Ltd, England, October 1989, No. 306;

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450 on 7-14-03.

Dated: 7-14-03



PHYLLIS de LANGIS

2. Jarvela, et al., "MLC DESIGN TO LIMIT SOFT ERROR FAILS", IBM Technical Disclosure Bulletin, Vol. 27, No. 2, July 1984, pp. 1343-1344;
3. Geppert, et al., "CMOS DRAM DESIGN LAYOUT TO IMPROVE SOFT ERROR IMMUNITY", IBM Technical Disclosure Bulletin, Vol. 34, No. 4B, September 1991, pp. 277-28; and
4. Dai, et al., "Alpha-SER Modeling & Simulation for Sub-0.25 μ m CMOS Technology", 1999 Symposium on VLSI Technology Digest of Technical Papers, pp. 81-82.

Applicants are submitting copies of the above-cited references.

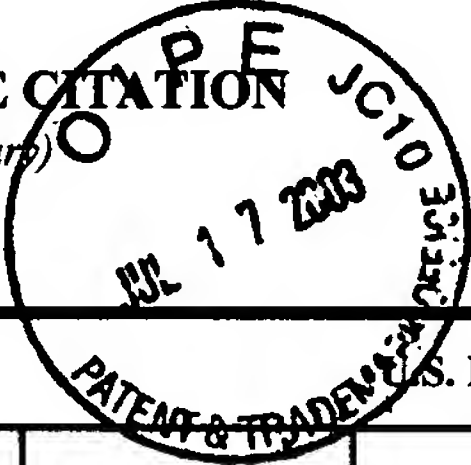
Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. §1.97(b), no petition, certification or fee is required.

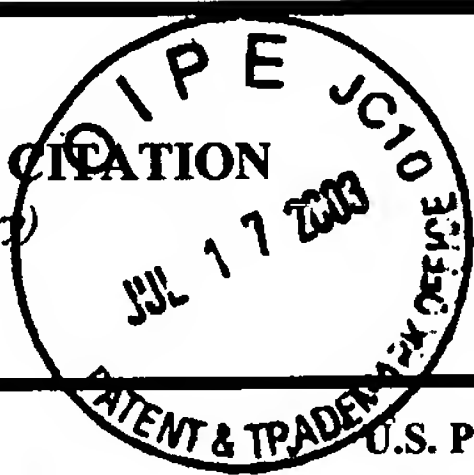
Respectfully submitted,


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<div style="display: flex; justify-content: space-between;"><div>INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i></div><div style="text-align: center;"></div></div>				Docket Number (Optional) BUR920010207US1 (15821)		Application Number 10/604179		
				Applicant(s) Kerry Bernstein, et al.				
				Filing Date 6-28-03		Group Art Unit Unassigned		
U.S. PATENT DOCUMENTS								
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
		Chan, "Technique for Reducing Personalized Array Soft Errors", RESEARCH DISCLOSURE, Kenneth Mason Publications Ltd, England, October 1989, No. 306						
		Jarvela, et al., "MLC DESIGN TO LIMIT SOFT ERROR FAILS", IBM Technical Disclosure Bulletin, Vol. 27, No. 2, July 1984, pp. 1343-1344						
EXAMINER				DATE CONSIDERED				
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